FLASH MEMORY WITH RDRAM INTERFACE

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This is a divisional application of application Serial No. 09/943,399, titled FLASH MEMORY WITH RDRAM INTERFACE, filed August 30, 2001, ~~(allowed)~~, now Patent No. 6,741,497 which application is assigned to the assignee of the present invention and the entire contents of which are incorporated herein by reference.

FIELD OF THE INVENTION

[0002] The present invention relates generally to memory devices and in particular the present invention relates to a non-volatile flash memory interface.

BACKGROUND OF THE INVENTION

[0003] A typical Flash memory comprises a memory array that includes a large number of memory cells arranged in row and column fashion. Each of the memory cells includes a floating gate field-effect transistor capable of holding a charge. The cells are usually grouped into blocks. Each of the cells within a block can be electrically programmed in a random basis by charging the floating gate. The charge can be removed from the floating gate by a block erase operation. The data in a cell is determined by the presence or absence of the charge in the floating gate.

[0004] A synchronous DRAM (SDRAM) is a type of DRAM that can run at much higher clock speeds than conventional DRAM memory. SDRAM synchronizes itself with a CPU's bus and is capable of running at 100 MHZ, about three times faster than conventional FPM (Fast Page Mode) RAM, and about twice as fast EDO (Extended Data Output) DRAM and BEDO (Burst Extended Data Output) DRAM. SDRAM's can